REMARKS

Claims 6-11 are pending in this application. Claims 6-11 have been rejected. Claims 6 and 9 have been amended to place the application in form for allowance. Applicants respectfully request allowance of pending claims 6-11.

In response to the various paragraphs of the Office action, applicants offer the following specific remarks in support of the patentability of the claims of the present application.

I. Rejection of Claims 6-11 under 35 USC §112, 2nd Paragraph

In the Office action, specifically in paragraph 3, claims 6-11 were rejected under 35 USC §112, 2nd Paragraph, as being indefinite. Applicants respectfully submit that these claim rejections are overcome based on the claim amendments and the remarks set forth below.

Each of originally filed claims 6 and 9 include the feature that the insulative layer has a dielectric constant greater than 5 "relative to free space". The Office action states that it is unclear as to how a dielectric constant can be greater than a space. Responsive to this rejection, claims 6 and 9 have been amended to excise the limitation of "relative to free space." As amended, each of claims 6 and 9 now recite the feature that the insulative layer has a dielectric constant greater than 5. Applicants respectfully submit that the term "dielectric constant" is well known in the art and does not require further definition in the claims. The dielectric constant is defined as "the ratio of the capacitance of a capacitor filled with a given dielectric to that of the same capacitor having only a vacuum as dielectric" in the McGraw-Hill Multimedia Encyclopedia of Science and Technology, for example.

As amended, each of independent claims 6 and 9 now comply with the requirements of 35 USC §112, 2nd Paragraph. Therefore, the rejection of claims 6 and 9 under 35 USC §112, 2nd Paragraph should be withdrawn. Claims 7 and 8 each depend directly from amended claim 6 and claims 10 and 11 each depend directly from amended claim 9. Therefore, the rejection of claims 7, 8, 10 and 11 under 35 USC §112, 2nd Paragraph, should also be withdrawn.

II. Rejection of Claims 6-7 and 9-11 under 35 USC §103(a)

In the Office action, specifically in paragraph 5, claims 6-7 and 9-11 were rejected under 35 USC §103(a) as being unpatentable over Yu (U.S. Patent No. 6,194,748). Applicants respectfully submit that these claim rejections are overcome based on the claim amendments and the remarks set forth below.

Claims 6 and 9 are independent claims, claim 7 depends from claim 6, and claims 10 and 11 depend from claim 9. Independent claim 6 has been amended to more definitely point out the present invention, as above. Amended claim 6 also includes the following distinguishing structural features:

> "an amorphous insulative layer having a dielectric constant greater than five",
>
> "a self-aligned source region",
>
> "a self-aligned drain region",
>
> "said gate structure, source region and drain region configured to form an operable self-aligned field effect transistor", and
>
> "said source region and said drain region directly self-aligned with the gate structure."

Amended independent claim 9 recites the following distinguishing structural features:

> "an amorphous insulative layer having a dielectric constant greater than 5",
>
> "a self-aligned source region and a self-aligned drain region, each . . . directly self-aligned with the gate structure", and
>
> "a self-aligned field effect transistor characterized by a gate leakage current less than 0.1 amp per cm^{-2} during operation."

It is **because** of various distinguishing aspects of the present invention, that the above-cited distinguishing structural features are achievable in combination. More particularly, it is because of the spatially selective annealing process of the present invention that the claimed structure formed according to the present invention enjoys the advantage of having a desirably

high dielectric constant, a self-aligned gate structure, and an operable field effect transistor, the combination of these features not being achievable according to the prior art.

The Examiner concedes that Yu does not teach source and drain regions being formed self-aligned with the gate structure. The Examiner then alleges that source and drain regions self-aligned with the gate structure are processing limitations and that a distinct structure is not necessarily produced. Applicants respectfully disagree with the Examiner's contention. Applicants respectfully point out that it is well known in the art that a self-aligned source and drain region, also referred to as a self-aligned gate of a transistor, is a distinguishing <u>structural</u> feature of a semiconductor device. Only <u>self-aligned</u> gate structures provide source/drain regions which are essentially perfectly aligned with respect to the gate structure, includes desirable dopant profiles only achievable using the transistor gate as a mask, and therefore includes a structurally distinguished channel region beneath the gate structure. The distinguishing channel region of a self-aligned gate is superior to a channel region formed by other means. The distinguishing advantages of a self-aligned transistor is explained in Wolf, "Silicon Processing for the VLSI Era," Volume 2, Lattice Press, on p. 318, for example. As such, a self-aligned gate structure is a <u>distinguishing structural feature</u> included in independent claims 6 and 9 and not taught in the cited reference of Yu, as conceded by the Examiner. Claims 6 and 9 have each been amended to actively recite a self-aligned source region, a self-aligned drain region and a self-aligned field effect transistor. As such, claims 6 and 9 are distinguished from the cited reference of Yu.

Furthermore, amended claims 6 and 9 are further distinguished from Yu because they each recite the feature that the source region and the drain region are <u>directly</u> self-aligned with the gate structure. Yu includes source/drain <u>extension regions</u> 23, 25, such that source/drain regions 22 and 24 are **not** directly aligned with the gate structure 18.

Within the art of field effect transistor fabrication, the art teaches that, in order to be <u>operable</u>, the source and drain regions of a transistor must be annealed at an elevated temperature after the source/drain regions are initially formed. This annealing process utilizes an elevated temperature high enough to activate the dopant impurities, cure the defects associated with introducing impurities into a substrate, and to achieve the desired dopant profile. According to the conventional art for producing a self-aligned source and drain region,

and in which the gate structure is used as a mask to form the self-aligned source and drain structures, the self-aligned source/drain regions are necessarily formed after the gate structure, including the gate dielectric and gate electrode, is intact. This means that the annealing process necessary to achieve the desired dopant characteristics, is necessarily carried out after the gate structure including any originally high-K insulative material, is formed using conventional technology. Typical annealing processes are carried out at a temperature of about 1000° C. Such an annealing process, necessary to produce source/drain regions required by an operable field effect transistor, will necessarily convert an amorphous insulative layer, already formed in the transistor gate, to a crystalline or polycrystalline structure and will therefore also lower the dielectric constant of an insulative material which may have been initially formed as a high-K dielectric material. After being exposed to the elevated temperatures typically used for annealing processes, an originally amorphous, high-K dielectric material will necessarily be converted to a crystalline material having a dielectric constant less than five. As such, according to the prior art, a self-aligned source and drain structure and an amorphous, high-K dielectric, are mutually exclusive in an operable transistor device (i.e., including annealed source/drain regions). The advantage of the present invention is that the spatially selective annealing process allows for annealing the self-aligned source and drain regions without converting the amorphous high-K dielectric material to a crystalline film having an undesirably low dielectric constant. This advantage produces the claimed structural advantages of an amorphous high-k insulative layer and self-aligned source and drain regions in a operable field effect transistor, as recited in amended claims 6 and 9

Amended claims 6 and 9 are therefore distinguished from the prior art. Furthermore, Applicants respectfully submit that one of ordinary skill in the art would not suggest simply ***not*** annealing the transistor structure because, as above, because the un-annealed source/drain regions would render the resulting transistor structure inoperable.

As conceded by the Examiner, the cited reference of Yu does not teach the structure including source regions and drain regions which are self-aligned with the gate structure, i.e. a self-aligned gate structure. The cited reference of Yu therefore does not teach or suggest any method for forming a self-aligned gate structure. Moreover, Applicants respectfully submit that the cited reference of Yu teaches away from using or forming a self-aligned gate. Yu

teaches first forming source and drain regions and source and drain extensions in the substrate first, then, after all high temperature processes are completed, forming the high-K insulative material over the gate region. The cited reference of Yu cautions against performing any high temperature processing operations after layer 34 - the high-K dielectric, is formed. As such, Yu teaches away from forming a self-aligned gate structure because a self-aligned source/drain structure is necessarily formed after the gate structure, including high-k dielectric layer 34, is intact and the annealing process which is necessarily carried out afterwards to provide an operable device, is a high temperature operation which Yu cautions against using after the high-k dielectric layer 34, is formed.

As such, each of amended independent claims 6 and 9 include features neither taught nor suggested by the cited reference of Yu. Claims 6 and 9 are each therefore distinguished from Yu and the rejection of claims 6 and 9 under 35 USC §103(a), should be withdrawn. Claim 7 depends from claim 6 and claims 10 and 11 depend from claim 9 and therefore the rejection of claims 7, 10, and 11 under 35 USC §103(a) as being unpatentable over Yu, should also be withdrawn.

III. Rejection of Claim 8 under 35 USC §103(a)

In the Office action, specifically in paragraph 6, claim 8 was rejected under 35 USC §103(a) as being unpatentable over Yu (as above) in view of Endo (U.S. Patent No. 5,596,214). Applicants respectfully submit that this rejection of claim 8 is overcome for the reason set forth below.

The cited reference of Endo has apparently been relied upon for disclosing a silicon oxide layer disposed between the insulative layer and the surface region. The cited reference of Endo therefore does not make up for the deficiencies of the primary reference of Yu. Since amended independent claim 6, the base claim from which dependent claim 8 depends, is distinguished from Yu for reasons set forth above, dependent claim 8 is therefore also distinguished from the cited reference of Yu. Since the cited reference of Endo does not make up for the deficiencies of Yu, dependent claim 8 is therefore distinguished from the references of Yu and Endo, taken alone or in combination. Therefore, the rejection of claim 8 under 35 USC §103(a) as being unpatentable over Yu in view of Endo, should be withdrawn.

Application No. 09/516,004

CONCLUSION

For the foregoing reasons, each of claim 6-11 are now in allowable form and the application is therefore in condition for allowance.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with Markings to Show Changes Made**."

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By ______________________
Mark J. Marcelli
Reg. No. 36,593
626/795-9900

MJM/mee

VERSION WITH MARKINGS TO SHOW CHANGES MADE

6. (Amended) An integrated circuit comprising:

a semiconductor material of a first conductivity type having a surface region for formation of devices;

a field effect transistor gate structure formed on the surface region, comprising a conductive layer and an amorphous insulative layer having a dielectric constant greater than five [~~relative to free space~~], the insulative layer formed between the conductive layer and the surface region;

a self-aligned source region formed along the surface region and having a second conductivity type; and

a self-aligned drain region formed along the surface region and having a second conductivity type, said gate structure, source region and drain region configured to form an operable self-aligned field effect transistor, said source region and said drain region directly self-aligned with the gate structure.

9. (Amended) A semiconductor device comprising:

a semiconductor material of a first conductivity type having a surface region for formation of devices;

a field effect transistor gate structure formed on the surface region, comprising a conductive layer and an amorphous insulative layer having a dielectric constant greater than 5 [~~relative to free space~~], the insulative layer formed between the conductive layer and the surface region; and

a self-aligned source region and a self-aligned drain region, each formed in the surface region, directly self-aligned with the gate structure and on a different side of the gate structure,

said gate structure, source region and drain region configured to form a self-aligned field effect transistor characterized by a gate leakage current less than 0.1 amp per cm^{-2} during operation.